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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2006 and 04 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on March 31, 2006 and August 4, 2006. Claims 1-4 of the application were amended. Claims 1-4 of the application are pending. This office action is made non-final.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-4 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

3.1 Amended claim 1 states in part, "wherein, for at least one circuit of said plurality of circuits, said library further comprises **logical delay operation information**, wherein **delay amounts** are provided for a signal transmission from input terminals to output terminals of a

logical circuit and wherein a **delay amount** is specific to an input terminal logical state transition and resulting logical state transition at an output terminal".

The specification does not describe anywhere the **logical delay operation information**. It also does not describe that the library comprises information wherein **delay amounts** are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a **delay amount** is specific to an input terminal logical state transition and resulting logical state transition at an output terminal. The specification only describes the **logical operation information** and **delay information** for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information.

The **logical delay operation information, delay amount** and their definition are ***new material*** not found in the original specification and therefore this amendment is not allowed.

3.2 Amended claim 2 states in part, "wherein, for each of said plurality of circuits, said library further comprises **logical delay operation information**, wherein **delay amounts** are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a **delay amount** is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of said plurality of circuits".

The specification does not describe anywhere the **logical delay operation information**. It also does not describe that the library comprises information wherein **delay amounts** are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a **delay amount** is specific to an input terminal logical state transition and resulting

logical state transition at an output terminal. The specification only describes the **logical operation information** and **delay information** for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information.

The **logical delay operation information, delay amount** and their definition are ***new material*** not found in the original specification and therefore this amendment is not allowed.

3.3 Amended claim 3 states in part, "said delay analysis library comprising connection information, delay time information and **logic operation delay information**, wherein **delay amounts** are provided for a signal transmission from input terminals of a logical circuit and wherein a **delay amount** is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits".

The specification does not describe anywhere the **logical operation delay information**. It also does not describe that the library comprises information wherein **delay amounts** are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a **delay amount** is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits. The specification only describes the **logical operation information** and **delay information** for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information.

The **logical operation delay information, delay amount** and their definition are ***new material*** not found in the original specification and therefore this amendment is not allowed.

3.4 Amended claim 4 states in part, "wherein, for at least one circuit of said plurality of circuits, said library further comprises **logical operation delay information**, wherein **delay amounts** are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a **delay amount** is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits".

The specification does not describe anywhere the **logical operation delay information**. It also does not describe that the library comprises information wherein **delay amounts** are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a **delay amount** is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of said plurality of circuits. The specification only describes the **logical operation information** and **delay information** for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information.

The **logical delay operation information, delay amount** and their definition are ***new material*** not found in the original specification and therefore this amendment is not allowed.

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites in part, "wherein said delay information for each signal path of the logical circuit of said at least one circuit is based upon ... ". There is insufficient antecedent basis for "said delay information for each signal path" in the claim.

Claim 2 recites in part, "wherein said delay information for each signal path of said at least one circuit is based upon logical state transitions at said input terminals and corresponding logical state transitions at said output terminals corresponding to logical operation information for said at least one circuit". There is insufficient antecedent basis for "said delay information for each signal path" and "said at least one circuit" in the claim.

Claim 3 recites in part, "wherein said delay information for each signal path of the logical circuit of said at least one circuit is based upon ... ". There is insufficient antecedent basis for "said delay information for each signal path" in the claim.

Claim 4 recites in part, "wherein said delay information for each signal path of the logical circuit of said at least one circuit is based upon ... ". There is insufficient antecedent basis for "said delay information for each signal path" in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Blinne et al.** (U.S. Patent 5,274,568) in view of **Hasegawa** (U.S. Patent 6,041,168) and further in view of **Hasegawa** (U.S. Patent 5,528,511).

8.1 **Blinne et al.** teaches method of estimating logic cell delay time. Specifically, as per Claim 1, **Blinne et al.** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach that for at least one circuit of the plurality of circuits, the library further comprises logical delay operation information. **Hasegawa** '168 teaches that for at least one circuit of the plurality of circuits, the library further comprises logical delay operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Blinne et al.** with the system of **Hasegawa** '168 that included for at least one circuit of the plurality of circuits, the library further comprising logical delay operation information, because delay verification time could be shortened and high speed delay verification achieved by calculating delay time based on logic information, connecting information and delay information (Col 2, Lines 28-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach that delay amounts are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a delay amount is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information. **Hasegawa** '511 teaches that delay amounts are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a delay amount is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay information for each signal path of the logical circuit of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to

logical operation information (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Blinne et al.** and **Hasegawa** '168 with the system of **Hasegawa** '511 that included delay amounts provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a delay amount was specific to an input terminal logical state transition and resulting logical state transition at an output terminal, and wherein the delay information for each signal path of the logical circuit of the at least one circuit was based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information, because this would provide correct delay time even when either of rise or fall of the signal had no effect in a delay time computation process (Col 2, Lines 61-65).

8.2 As per Claim 2, **Blinne et al.** teaches the delay analysis system for making a delay analysis of a logic circuit (Col 1, Lines 7-13);

the system having a delay analysis library (Col 1, Lines 9-13); and

comprising connection information and delay time information for a plurality of circuits (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach that for each of the plurality of circuits, the library further comprises logical delay operation information. **Hasegawa** '168 teaches that for each of the plurality of circuits, the library further comprises logical delay operation information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach that delay amounts are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a delay amount is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of the plurality of circuits, and wherein the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information for the at least one circuit. **Hasegawa** '511 teaches that delay amounts are provided for a signal transmission from input terminals to output terminals of a logical circuit and wherein a delay amount is specific to an input terminal logical state transition and resulting logical state transition at an output terminal for each circuit of the plurality of circuits, and wherein the delay information for each signal path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals corresponding to logical operation information for the at least

one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

8.3 As per Claim 3, **Blinne et al.** teaches a method for making a delay analysis of a logic circuit (Col 1, Lines 7-13); comprising the steps of:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information, and delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach the delay analysis library comprising logic operation delay information. **Hasegawa** '168 teaches library comprising logic operation delay information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa** '168 do not expressly teach that delay amounts are provided for a signal transmission from input terminals of a logical circuit and wherein a delay amount is

specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay information for each path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by logical operation information for the at least one circuit. **Hasegawa** '511 teaches that delay amounts are provided for a signal transmission from input terminals of a logical circuit and wherein a delay amount is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay information for each path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Blinne et al. and **Hasegawa** '168 do not expressly teach if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information or if a selected output terminal transitions from a high state to a low state the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

8.4 As per Claim 4, **Blinne et al.** teaches a computer-readable medium having stored thereon a program comprising computer instructions that, when executed on a computer perform a process for executing a delay analysis method for a logic circuit, the computer readable medium causing a computer to execute the method (Col 2, Lines 42-50); wherein the method comprises:

referencing a delay analysis library for a plurality of circuits (Col 1, Lines 9-13);

the delay analysis library comprising connection information and delay time information (Col 1, Lines 39-40; Col 1, Lines 60-62; Col 1, Lines 45-48).

Blinne et al. does not expressly teach the delay analysis library comprising logic operation delay information. **Hasegawa** '168 teaches that the library comprising logical operation delay information (Col 1, Lines 58-61 and Col 2, Lines 31-35).

Blinne et al. and **Hasegawa** '168 do not expressly that delay amounts are provided for a signal transmission from input terminals of a logical circuit and wherein a delay amount is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay information for each path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by logical operation information for the at least one circuit. **Hasegawa** '511 teaches that delay amounts are provided for a signal transmission from input terminals of a logical circuit and wherein a delay amount is specific to an input terminal logical state transition and resulting logical state transition at each output terminal for at least one circuit of the plurality of circuits, the delay information for each path of the at least one circuit is based upon logical state transitions at the input terminals and corresponding logical state transitions at the output terminals as represented by logical operation information for the at least one circuit (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the

delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified).

Blinne et al. and **Hasegawa** '168 do not expressly teach if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected output terminal according to the logical operation information. **Hasegawa** '511 teaches if the logic circuit comprises the at least one circuit, selecting the delay time of each path of the at least one circuit from the delay time information, wherein if a selected output terminal transitions from a low state to a high state, the delay time is selected based on the input terminal whose logical transition triggers the low state to high state transition of the selected output terminal according to the logical operation information, or if a selected output terminal transitions from a high state to a low state, the delay time is selected based on the input terminal whose logical transition triggers the high state to low state transition of the selected

output terminal according to the logical operation information (CL1, L28-35; Col 2, Lines 30-42; Col 3, Lines 5-26).

Blinne et al. and **Hasegawa** '168 do not expressly teach performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit. **Hasegawa** '511 teaches performing a delay calculation to determine a propagation delay time using the selected delay time of the at least one circuit (Col 3, Lines 5-26).

Response to Amendments

9. Applicants' amendments, filed on March 31, 2006 have been considered. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive.

9.1 As per the applicants' argument that "Hasegawa `511 fails to teach a delay amount is specific to an input terminal logical state transition and resulting logical state transition at an output terminal as taught by the subject application; Blinne et al., Hasegawa `168 and Hasegawa `511 fails to teach or suggest either alone or in combination, a delay amount is specific to an input terminal logical state transition and resulting logical state transition at an output terminal", the examiner respectfully disagrees.

Hasegawa '511 teaches a delay amount is specific to an input terminal logical state transition and resulting logical state transition at an output terminal (Fig. 3; Col 1, Lines 28-35; Col 2, Lines 30-42; Col 3, Lines 5-26; Fig. 3 shows the logical state transitions at each input

terminal and logical state transitions at each output terminal; Col 1, Lines 28-35 discusses the logical state transitions at the input terminal and the output terminal, using rise/fall terms; Col 2, Lines 30-42 states that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid); it is clear that the logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit; Col 3, Lines 5-26 describes that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified), as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (Col 2, Lines 61-65).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
August 19, 2006